Amendments to the Specification:

Please replace paragraph [0017] with the following amended paragraph:

[0017] The semiconductor layer 12 can be applied in a polysilicon resistor or a diffusion resistor according to the present invention. When being applied in a polysilicon resistor, the polysilicon layer 12 is formed of polyslicon, and a dielectric layer ~~(not shown)~~ 13 is positioned underneath the semiconductor layer 12 to enable the semiconductor layer 12 to connect with other underneath wirings through contact plugs formed in the dielectric layer. When being applied in a diffusion resistor, the semiconductor layer 12 is a diffusion layer formed by doping dopants into the substrate 10, and an ion implantation well ~~(not shown)~~ 15 is positioned underneath the semiconductor layer 12 depending on electrical characteristics demands of the products.

Please replace paragraph [0018] with the following amended paragraph:

[0018] In a better embodiment of the present invention, the high resistance region A further includes a salicide block (SAB) 14 positioned on the semiconductor layer 12a and the portions of the semiconductor layer 12b adjacent to the junction between the high resistance region A and the low resistance region B. The low resistance region B further includes a salicide layer 16 positioned on portions of the semiconductor layer 12b. In addition, an ~~inter-layer~~ inter-layer dielectric (ILD) 18 is also formed on the substrate 10 to insulate the salicide layer 16 from other conductive materials. At least a contact hole 20 connecting to the salicide layer 16 is formed within the ~~inter-layer~~ inter-layer dielectric 18. At least a conductive layer 22 is formed on portions of the ~~inter-layer~~ inter-layer dielectric 18 and within the contact hole 20, thus connecting the resistor structure to wirings formed above the ~~inter-layer~~ inter-layer dielectric 18 via the conductive layer 22 filling in the contact hole 20.

Please replace paragraph [0020] with the following amended paragraph:

[0020] As shown in Fig. 4, after the removal of the mask 24, the salicide block 14 is formed on the semiconductor layer 12a and the portions of the semiconductor layer 12b within the high resistance region A. Using the salicide block 14 as a mask, the salicide layer 16 is formed on the portions of the semiconductor layer 12b within the low resistance region B to reduce the end-resistance of the semiconductor layer 12b. Subsequently, the ~~inter-layer~~ inter-layer dielectric 18, such as a silicon oxide layer or a borophosphosilicate glass (BPSG), is formed on the surface of the substrate 10 to insulate the salicide layer 16 from other conductive materials. Following that, a photolithographic process and an etching process are performed to form the contact hole 20 in the ~~inter-layer~~ inter-layer dielectric 18 to connect to the salicide layer 16. The conductive layer 22 is then formed on portions of the ~~inter-layer~~ inter-layer dielectric 18 and within the contact hole 20, thus connecting the resistor to wirings formed above the ~~inter-layer~~ inter-layer dielectric 18 via the conductive layer 22 filling in the contact hole 20.